

**CALL FOR PAPERS**

The logo for LATS 2020 features the word "LATS" in a teal, bold, sans-serif font, followed by "2020" in a yellow and orange gradient, bold, sans-serif font. The text is centered within a white, irregular, hand-drawn shape. The background of the entire page is a scenic photograph of a tropical beach with a blue sky, palm fronds, and a body of water.

# **LATS2020**

**21<sup>st</sup> IEEE Latin-American Test Symposium**

Jatiúca (Maceió), Brazil, 30<sup>th</sup> March - 2<sup>nd</sup> April 2020

[www.lats.tttc-events.org](http://www.lats.tttc-events.org)

# 21<sup>st</sup> IEEE Latin-American Test Symposium

Jatiúca (Maceió), Brazil, 30<sup>th</sup> March - 2<sup>nd</sup> April 2020



## CALL FOR PAPERS

The IEEE Latin-American Test Symposium (LATS) is a recognized test and fault tolerance techniques forum attended by professionals from all over the world, in particular from Latin-America, to present and discuss various aspects of system, board, and component testing as well as design, manufacturing and in-field considerations with fault tolerance in mind. All presented papers will be submitted to IEEE Xplore Digital Library and the best papers of its 21<sup>st</sup> edition will be invited to re-submit to IEEE Design&Test, Journal of Electronic Testing: Theory and Applications (JETTA - Springer), Journal of Low Power Electronics (JOLPE - American Scientific Publishers), and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).

## Topics of interest include but are not limited to

- Analog Mixed Signal Test
- Automatic Test Generation
- Built-In Self-Test
- Defect-Based Test
- Design and Synthesis for Testability
- Design for Electromagnetic Compatibility
- Design for Reliable Embedded Software
- Design Verification / Validation
- Economics of Test
- Fault Analysis and Diagnosis
- Fault Modeling and Simulation
- Fault-Tolerance in HW/SW
- Fault-Tolerant Architectures
- Memory Test and Repair
- On-Line Testing
- Process Control & Measurements
- Radiation / Electromagnetic Interference
- Hardening Techniques
- Software Fault-Tolerance
- Software On-Line Testing
- System-on-Chip Test
- Test Resource Partitioning
- Yield Optimization
- Hardware Security

## Paper Submission Information

To encourage and facilitate discussions, participation will be limited. Those interested in presenting recent results at the symposium are invited to submit an extended abstract, one to three pages long, or a full length paper. PDF electronic submissions must be done via the symposium's webpage: [www.lats.tttc-events.org](http://www.lats.tttc-events.org)

Authors should send papers in the IEEE format. Detailed instructions are available at the symposium's webpage. The Program Committee also welcomes proposals for panels and special sessions.

For additional information, please contact our Program Co-Chairs:

Victor Champac – INAOE, Mexico  
[champac@inaoep.mx](mailto:champac@inaoep.mx)

Tiago Balen, UFRGS, Brazil  
[tiago.balen@ufrgs.br](mailto:tiago.balen@ufrgs.br)

**Submission (Title&Abstract and Full paper): December 1<sup>st</sup>, 2019**

**Notification of Acceptance: January 15<sup>th</sup>, 2020**

**Camera Ready: January 29<sup>th</sup>, 2020.**

Maceió is the capital and largest city of the coastal state of Alagoas, Brazil. The name is indigenous for "spring". The cuisine in the area is amazing and lovers of good food will enjoy seafood, Italian cuisine, hamburgers, tapioca, couscous, and lots of other typical dishes. Jatiúca is one of Maceió's prime neighborhoods and shops for all tastes are easily found on the main avenues or inside a nearby mall.

The Jatiúca Beach is a great choice for your sea bathing, resting in the sand, surfing and walking along the waterfront. The landscape and the cosy climate inspire to enjoy your days. In addition to the relaxing ambience, Jatiúca offers a great structure: kiosks, bars, restaurants, ice cream parlors and cafes are what is not lacking here.

## Technical Sponsors:



The Institute of  
Electrical and Electronics  
Engineering, Inc.



Test Technology  
Technical Council

## Organized by:



PUCRS, Brazil

## Financial Sponsor:



IEEE Council on  
Electronic Design  
Automation

## General Co-Chairs:

Leticia Maria Bolzani Poehls – PUCRS, Brazil  
[leticia@poehls.com](mailto:leticia@poehls.com)

Yervant Zorian – SYNOPSYS, USA  
[yervant.zorian@synopsys.com](mailto:yervant.zorian@synopsys.com)

## Past General Chair:

Raoul Velazco - TIMA, France

## Vice General Chair:

Roberto Gomez - University of Sonora, Mexico

## Program Co-Chairs:

Victor Champac – INAOE, Mexico  
Tiago Balen - UFRGS, Brazil

## Vice Program Co-Chairs:

Pablo Ferreyra - University of Cordoba, Argentina  
Felipe Restrepo - Nat. Univ. of Colombia, Colombia

## Special Session Co-Chairs:

Fabian Vargas - PUCRS, Brazil  
Matteo Sonza Reorda - POLITO, Italy

## Publication Chairs:

Ernesto Sanchez Sanchez - POLITO, Italy

## Industry Liason:

Marcelo Lubazewski - UFRGS, Brazil  
Victor Grimblatt - Synopsys, Chile

## European Liason:

Hans-Joachim Wunderlich - Univ. Stuttgart, Germany

## Asian Liason

Stefan Holst - Kyushu Institute of Technology, Japan

## Fotos from Jatiuca and surroundings :



The city of Maceió



Palm trees at Gunga Beach



Rock formations at Gunga Beach

## Steering Committee:

Victor Champac - INAOE, Mexico  
Marcelo Lubazewski - UFRGS, Brazil  
Fabian Vargas - PUCRS, Brazil  
Raoul Velazco - TIMA, France  
Yervant Zorian - Synopsys, USA  
Tiago Balen - UFRGS, Brazil  
Leticia M. Bolzani Pöhls - PUCRS, Brazil  
Matteo Sonza Reorda - Politecnico di Torino, Italy